

Appn No. 10/727,227
Amtd. Dated August 15, 2005
Response to Office Action of July 18, 2005

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Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Original) An integrated circuit incorporating microelectromechanical systems (MEMS), having a total area greater than an area of at least one of the reticles used to manufacture it.
2. (Original) An integrated circuit according to claim 1, including a stitch region where the multiple reticle fields overlapped during manufacturing of the integrated circuit.
3. (Original) An integrated circuit according to claim 1 or 2, wherein the surface area of the integrated circuit is larger than a single stepping field of a reticle used to manufacture the integrated circuit.
4. (Original) An integrated circuit according to claim 2, manufactured using at least two different types of reticles.
5. (Original) An integrated circuit according to claim 2, manufactured using multiple applications of the same reticle.
6. (Original) A printhead integrated circuit according to claim 1.
7. (Withdrawn) A method of manufacturing an integrated circuit incorporating MEMS, comprising laying out the integrated circuit using a plurality of overlapping reticles.
8. (Withdrawn) A method according to claim 7, wherein the overlapping reticles are the same as each other.
9. (Withdrawn) A method according to claim 7, wherein the reticles are different to each other.
10. (Withdrawn) A method according to claim 9, wherein the reticles are different lengths.

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11. (Withdrawn) A method of manufacturing an integrated circuit printhead according to claim 7.

12. (Withdrawn) A method of manufacturing a plurality of integrated circuits on a single substrate wafer, wherein each of the integrated circuits is manufactured in accordance with claim 7.

13. (Withdrawn) A method according to claim 12, wherein at least some of the integrated circuits are different to each other.

14. (Withdrawn) A method according to claim 13, wherein the integrated circuits are of different lengths.

15. (Withdrawn) A method laying out an integrated circuit according to claim 1, the method including the steps of:

defining a layout of an integrated circuit;

defining a joint path;

modifying at least one element within an overlap area adjacent the joint path to take into account reticle field overlap during a subsequent manufacturing step.